Remarks:

This amendment is submitted in an earnest effort to advance this case to issue without delay.

The instant invention is aimed at quickly and efficiently producing a strained silicon layer on an SOI structure. This is an improvement on the known wafer bond method.

This goal is achieved by "dislocation mediated strain transfer," by which is meant that a layer overlying the silicon layer is relaxed so as to strain the silicon layer of the commercially available SOI substrate. This is a revolutionary advance in the field. It is unknown to transfer strain like this. The advantages in the production of semiconductors are enormous, as this is much faster than the wafer bond process.

Nothing like this is seen in the cited art. More particularly the rejection on Christiansen contains several fundamental errors:

Christiansen does not teach a "method of producing a strained layer (SiGe layer 410 in FIG. 13) on a substrate"... Christiansen teaches exclusively a method for relaxing an originally strained (SiGe) layer by ion implantation and annealing on a Si or SOI wafer. The strained layer (claim 48) is deposited on the relaxed (SiGe) layer (= the virtual substrate) after

relaxation, as many other groups have shown before on various types of virtual substrates.

Christiansen does not use or teach "strain transfer", since the strained Si layer is epitaxially deposited on the relaxed layer (layer 50 FIG. 13 and [0042-0046]: "A strained layer is deposited on layer 410").

Explanation: During epitaxial growth the in-plane lattice parameter of the deposited Si-layer adjusts to the (SiGe-)substrate and becomes strained. This process according to Christiansen allows the fabrication of a strained layer exclusively only on top of the virtual substrate.

The "dislocation mediated Strain transfer" according to the invention means something very different. With the instant invention, the thin silicon layer of the SOI substrate, which is underneath the relaxing layer, becomes strained during the relaxation process. This process is unique and uses dislocation transfer into a very thin layer to strain the layer.

In contrast, in Christiansen's approach the SiGe layer (e.g. layer 400 in FIG. 12) relaxes but the neighboring layer remains unchanged during this process, because the layers under the relaxing SiGe layer are far too thick and consist of several layers (10, 20, 30, 40) including the defect layer.

The differences between Christiansen and the instant invention can be broken down as follows:

1. Christiansen uses an SOI or Si Substrate whose layers remain unchanged.

The instant invention uses a thin Si layer and converts it into a strained Si layer.

2. Christiansen epitaxially grows a stack of layers.

The instant invention grows a single epitaxial layer on a layer to be strained.

3. Christiansen implants ions through the relaxing layer to form a defect layer (30 in FIG. 12). This damages the relaxing layer.

The instant invention implants ions into the top layer (4, 5) or defect layer above the SOI substrate. No damage to lower part of the relaxing or additional layer.

4. Christian anneals so the SiGe layer relaxes.

With the instant invention the SiGe layer is relaxed so as to strain the underlying layer.

5. Christian puts strained Si on a virtual substrate with a thickness of about 300 nm on oxide (FIG. 12).

With the instant invention the strained Si is formed directly on the insulating oxide.

6. To make a strained silicon on insulator Christiansen removes the layer stack by selective etching.

The instant invention only etches off the relaxed layer.

7. Further, Christiansen requires numerous extra steps, namely:

Epitaxial deposition of a strained Si layer.
Smart cut hydrogen implantation.
Oxide deposition, deposition, wafer bonding,
Wafer splitting during heating and polishing.

In summary, Christiansen's method does not allow the fabrication of a strained layer directly on oxide without wafer bonding in contrast to our claims 1, 97, and 98.

A further comparison shows the fundamental differences of resulting device structures as suggested by Christiansen in FIG. 18 and by our approach FIG. 9 (see FIG. below). Christiansen's method suffers from severe drawbacks: Devices (MOSFETs, MODFETs etc.) or layered structures (Christiansen FIG. 18-22) can only be realized ON TOP of the virtual substrate, which consists of many layers (20,30,40, 400).

In Christiansen as shown in FIG. 18 the strained layer 50 is on top of the layers 20, 30, 40 and 400 (SiGe), so that such important devices as fully depleted MOSFETs cannot be made. These parasitic layers have a total thickness of about 400 nm or more. As a consequence, the intrinsic advantages of the expensive SOI substrate (5, 10, 20) cannot be fully exploited. The transistors cannot be isolated by shallow trench isolation (STI) in contrast to FIG. 9 of our approach.

With the instant invention the strained layer 9 (and 3), forms the channel of a fully depleted MOS transistor, since the

layer is directly on the insulating SiO2 (layer 2). Standard "shallow trench isolation" (14) can be easily employed to isolate the transistors on the oxide (layer 2).

Furthermore Christiansen's various proposed patterning approaches or the multiple repetition of the implantation/annealing process in multiple layer structures do not eliminate these severe disadvantages.

The examiner's statement with respect to claim 10 contradicts fundamental physics because "weight of a layer" is an inappropriate term, since neither the physical weight of a layer nor the stress of layer leads to strain transfer to the neighboring layer, simply because the stress is taken up by the "infinitely" thick substrate. (To be more precise: The stress of a thin layer may cause wafer bending and thus to a very, very small strain in the neighboring layers. This effect, however, is much too small to be used and is not addressed here.)

It is important to note that this misunderstanding led to several erroneous conclusions such as (office action, page 10, paragraph 41 and page 9, paragraph 39). More particularly, Brasen uses a standard approach for the growth of a strained layer on relaxed thick, graded SiGe layer (with several additional layers) in a thickness range of 2 to 10 micrometers and shows the benefit of a strained layer for the fabrication of MODFETs (FIG. 2) and

LED's. Brasen describes the fabrication of these devices on the thick virtual substrate on a bulk silicon wafer. The examiner refers to a defect layer (2) in Brasen's patent and constructs similarities to our application, ignoring that the defects in Brasen's approach result from the growth of the lattice mismatched layer stack (virtual substrate) and that their density, their character and there spatial extensions are completely different from the defects produced by ion implantation. With other words, the defects addressed by Brasen are not suitable to induce or support "strain transfer." Furthermore, it is worth mentioning that Brasen neither makes use of "strain transfer" nor uses SOI as done in the instant invention. The only oxide layer Brasen mentions is the gate oxide layer.

Brasen does not teach or suggest the making of a strained layer directly on oxide. Therefore, the combination of Christiansen and Brasen also does not provide any information in this respect.

Like Christiansen and Brasen, Imai grows a strained Si layer (16) on a partially relaxed SiGe layer (15) by epitaxial deposition. Again, the strained layer is not produced by "dislocation mediated strain transfer" nor is the layer on an oxide. Imai deposits an amorphous 200 nm SiGe layer with 30 at% Ge on an oxidized Si bulk wafer after etching an opening in the oxide. In a second step the SiGe is recrystallized at 600°C (column 8,

line 28ff). Severe disadvantages of this approach are obvious. First, recrystallisation of SiGe does not lead to high quality layers and, second, the degree of relaxation is very small. Furthermore, this method can be used, if at all, only locally and not for full wafers.

In conclusion, Imai's approach is technically extremely limited and neither allows the making of a homogenous strained layer on a full wafer nor a strained layer directly on an oxide.

In column 9, lines 26-34 Usuda describes the process and again the examiner misunderstands the explanation. Usuda uses hydrogen-ion implantation and annealing (well known as the "SMART CUT process") to delaminate the film from the substrate. When the substrate is removed elastic strain sharing (without dislocations) between the delaminated layers will occur. Subsequently, Usuda employs wafer bonding in order to obtain a strained layer on top of an oxide. Usuda's process, however, suffers from severe difficulties. If the film delaminates from the substrate before wafer bonding the film would roll up and become useless. Therefore, wafer splitting (heating of the hydrogen implanted wafer) is done after bonding. As soon as the bond strength increases during heating, the film is no longer free standing and the strain sharing process stops. In other words, the strain buildup in the Si layer is very small. This process is technologically laborious and a successful demonstration has not

been shown as yet. Usuda describes various sample structures which could be used for layer transfer in a wafer bonding process.

In summary, wafer bonding is an alternative route to produce strained Si directly on an oxide, however, wafer bonding is an expensive and complex technology as compared with our approach.

Jerome teaches the fabrication and advantages of a conventional SOI Substrate for making bipolar transistors used at high voltages. Naturally, the buried oxide has inherent advantages with respect to electrical isolation and parasitic capacitances. Jerome's focuses on electrical effects. Jerome neither addresses the use of a strained layer or a strained heterostructure nor does he deal with defect engineering in epitaxial heterostructures. Also the presented devices with many micron thickness have no similarities with devices as shown in FIG. 9 of the instant invention. Hence, Jerome provides not the slightest hint how to fabricate a strained layer on an oxide.

Dhaka describes a process for fabricating a MOSFET device on a conventional bulk substrate. He proposes a specific mask technique for making source and drain regions. Dhaka neither uses strained layers nor produces any. No SOI substrate is even used. Any relation or even a hint with respect to our application cannot be seen.

Claim 73 relates to the reduction of the surface roughness. Oxidation helps to reduce the roughness in the sub-nanometer range. The examiner suggests "filling layers into gaps caused by uneven surface" and further he refers to layer peeling. These suggestions are inapposite.

For these reasons the instant invention is clearly allowable over the cited art. Notice to that effect is earnestly solicited.

If only minor problems that could be corrected by means of a telephone conference stand in the way of allowance of this case, the examiner is invited to call the undersigned to make the necessary corrections.

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